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**Complete if Known**

Application Number	10/533,141
Filing Date	April 27, 2005
First Named Inventor	Jun-ichi Okamura
Art Unit	Confirmation No. 5031 — 2816
Examiner Name	DIANA CHENG
Attorney Docket Number	1032-0002WOUS

Sheet 2 of 2

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
/DC/		James H. Atherton and H. Thomas Simmonds, "An Offset Reduction Technique for Use with CMOS Integrated Comparators and Amplifiers", 8107 IEEE, 08/27/92; New York, US	

Examiner Signature	/Diana Cheng/	Date Considered	06/09/2007
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27 APR 2005

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10/533141

[illegible]

Jun-ichi Okamura

2816

Diana Chen

1032-0002WOUS

Sheet	1	of	1
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.†	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T
		Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>6</sup> (if known)				
/DC/		JP 7-58872 B2	06-21-95	Toshiba		✓
/DC/		JP 7-193439 A	07-28-95	Fujitsu		✓

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